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ARSTRACT (Continue on reverse side if necessary and identity by block number)

Research performed was directed at understanding the effects of ion implantation on the radiation hardness of the SiO gate oxide of MOS devices. MOS capacitors were used as test structures and capacitance-voltage measurements were combined with photoinjection, photodepopulation, thermal annealing and variable temperature measurements on both implanted and unimplanted samples

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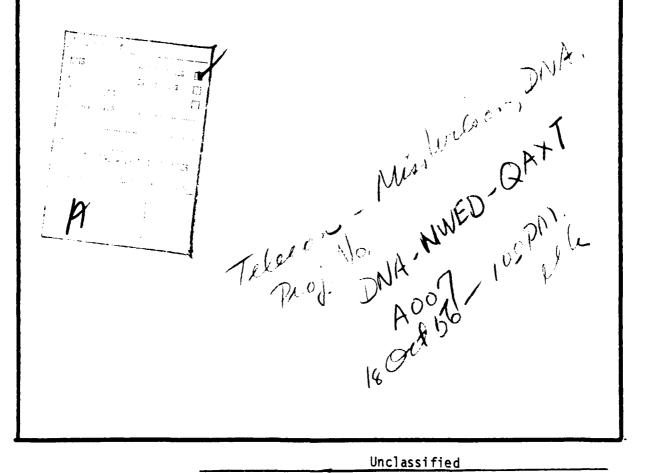
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in order that the modified oxide charge trapping could be probed. measurements were made using the scanning electron microscope as a source of electrons of controlled energy. C-V and G-V data was taken with the MOS samples in the microscope environment, the beam energy being slowly increased to probe the oxide to increasing depths.

The experimental data indicates that the primary effect of the implantation process is to produce electron traps associated with the implantation induced displacement damage. At room temperature, electrons in these traps can charge compensate holes trapped near the Si/SiO_2 interface. At low temperatures however, the increased hole trapping at this interface overcomes the effects of the trapped electrons and dominates the flat band voltage shifts.

A model of the charge trapping behavior has been developed which satisfactorily explains the observed behavior.



THE STABILITY OF DIELECTRIC COATINGS UNDER RADIATION

I. INTRODUCTION

Metal-Oxide-Semiconducting structures are becoming increasingly important in large scale integrated circuits for data processing and memory uses and in charged coupled devices used as solid state imaging systems. In the ideal system the oxide is an inert insulator separating the metal gate electrode from the semiconducting substrate. In satellite applications, MOS structures are exposed to an ionizing radiation environment and the insulator is no or injected into it from the metal gate electrode and the semiconducting substrate. Some of these carriers become trapped in the oxide, altering the field at the silicon surface and hence the operating threshold of the device. This charge storage can take the threshold out of the range available from the power supplies associated with the circuits or cause power consuming leakage currents. If the device is operated at low temperatures, such as may be desirable in a sensitive infrared solid state imaging system, the trapping of positive charges in the oxide is greatly increased and image deterioration occurs at total doses as low as 104 rads (Si).

Three approaches have been used in an attempt to improve oxide behavior in a radiation environment: (1)

- (a) Strict control of the conditions under which the SiO₂ is grown, including the surface preparation of the Si and freedom from ionic contaminants such as Na.
- (b) Modifications of SiO₂, produced under the conditions determined in (a), by ion-implantation with Al or the diffusion of chromium into the oxide.
- (c) The use of a gate insulator other than SiO_2 , with Al_2O_3 being the favored alternative.

This report is concerned with experiments that have been made on Al implanted, SiO₂ insulated MOS capacitor structures in order to understand the changes in oxide charge storage produced by the implantation, the thermal

stability of the oxide modifications and their spatial distribution within the oxide. The techniques of photoinjection, photodepopulation, and capacitance-voltage measurements have been used to determine the electronic trap structure of both implanted and unimplanted SiO₂ and its response to ionizing radiation. The scanning electron microscope has been used as a source of radiation with a controlable penetration into the oxide as well as an imaging system. The results of studies on samples implanted at different energies and of thermal annealing experiments are discussed below and a simple model is presented which explains the observed equilibrium charge storage behavior under both positive and negative gate bias conditions.

The data presented indicates that ion implantation is a suitable technique for controling the radiation hardness of MOS structures at room temperature. The low temperature data, however, indicates that the compensatory electron traps introduced by the ion implantation process are not able to compensate for the increased interfacial hole trapping that occurs at liquid nitrogen temperatures. Alternate methods are therefore needed to increase the hardness of CCD's used as low temperature imaging devices.

II. EXPERIMENTAL

In order to determine the effects of implantation and thermal annealing on the electrical behavior of MOS systems, measurements were made on the charge storage in both unimplanted and implanted MOS capacitors as a function of X-ray dose, sample temperature, bias during irradiation and annealing history. The oxides used were grown on $3\Omega \text{cm} < 100 > \text{n-type}$ silicon to a thickness of 1315 + 20 Å by dry oxidation at Hughes Aircraft⁽²⁾. The Al⁺ implantation was with 10^{14} or 10^{15} ions cm⁻² at 10, 20 or 30 KeV. On the basis of ion microprobe measurements⁽³⁾ the 20 KeV implantation is known to produce an Al⁺ ion distribution with its peak between 200 and 500 Å from the gate electrode. Either semi-transparent gold or opaque aluminum gate electrodes were vacuum evaporated onto the samples. The gold electrodes had a thickness of about 150 Å and enabled photodepopulation methods to be used to study the charge trapped after X-irradiation.

For the measurements discussed below each sample was mounted on the cold finger of a vacuum cryostat and could be subjected to various experimental probes. The apparatus has been previously described (4). The sample temperature could be controlled in the range between 80 and 300°K and all measurements could be made at any temperature.

X-irradiation of the sample was performed at 90 KeV, 20mA with a tungsten target tube. The estimated dose rate at the sample was 10⁶ rads (Si) per hour. Light for the photodepopulation studies came from a Xenon source used in conjunction with wide band filters. The charge state of the capacitor was determined using Capacitance-Voltage (C-V) techniques (5) with the flat band voltage condition being used to provide a measure of the charge stored in the oxide and in interface states. A Boonton Model 72B Capacitance meter was used to measure the small signal capacitance at a frequency of 1 MHZ in conjunction with a voltage ramp that could be varied between 0.01V/sec and 10V/sec. Thermal annealing was performed in a vacuum furnace of low thermal inertia with the sample held between sapphire plates. The furnace and the plates were specially cleaned to minimize any uptake of sodium during the annealing process. Both isochronal and isothermal annealing measurements were made. Some samples were mounted on the specimen stage of a scanning electron microscope developed at Princeton. The microscope specimen chamber was modified to allow electrical interaction with the specimens and C-V and G-V measurements were made on capacitor samples within the microscope after various exposures to the electron beam. Samples were held under a constant bias of +10 volts with the gate electrode at ground potential. The electron beam current was maintained at 10⁻⁸ amps and the samples exposed for periods of 15. 30. 60 and 120 seconds at various beam energies between 500 and 4000 eV. The electron beam energy was increased in 100 volt steps after each exposure series and the chosen energy range corresponded to electrons stopping in the gate electrode, the oxide and, at the highest energy, in the silicon substrate. A minicomputer was coupled to the measuring apparatus and used to compute the interface state density after each exposure.

III. RESULTS

a. The Unimplanted Oxide.

Extensive measurements have been made of the behavior of unimplanted oxide samples exposed to ionizing radiation at both room temperature and liquid nitrogen temperature. These results have been previously reported (6). Figure 1 summarizes the saturated flat band voltage behavior of a typical sample exposed to X-rays at either room temperature or liquid nitrogen temperature. The data points were obtained by setting the desired gate voltage and exposing the capacitor to X-irradiation for approximately 3 hours. The saturated flat band voltage shift was then measured, the gate voltage changed to the next value and the radiation exposure continued for a similar time. Each data point therefore represents an additional 3 x 10 rads (Si) of irradiation with respect to the previous point. The gate voltage on the specimen was varied in a random way for each run. The saturated flat band voltage, V(sat), depends upon the temperature and the bias on the sample during X-irradiation but is independent of the flat band voltage condition at the beginning of an exposure (7).

It is seen that the unimplanted oxide has a net positive charge storage for both gate bias polarities at room temperature and at liquid nitrogen temperature. At liquid nitrogen temperatures the oxide stored less positive charge under negative bias than under the corresponding bias at room temperature. For positive gate voltages up to about 10 volts considerably more positive charge was stored in the oxide at 80°K than at room temperature. Photodepopulation studies indicated that this additional charge was in different traps from those associated with room temperature hole trapping since it could be removed by photons with an energy of circa 2.5 eV, whereas the charge stored in the room temperature stable traps could not be photodepopulated 16°C. These additional traps are close to the Si/SiO2 interface and may be emptied by field emission processes.

b. The Implanted Oxide

Figure 2 shows the corresponding saturated flat band voltage shift as a function of gate voltage during X-irradiation for the implanted oxide samples.

Under negative bias conditions the charge storage was very similar to that in the unimplanted oxide, with V(sat) having a linear dependence on V at both 80°K and room temperature and indicating net positive charge storage in the oxide. Under positive gate voltage conditions the behavior at room temperature was quite different from that of the unimplanted oxide. V(sat) was positive, corresponding to net negative charge storage in the oxide, for X-ray doses of circa 3 x 10° rads (Si). The value of V(sat) under these positive gate voltage conditions was also found to depend upon the energy of Al^+ implantation. Values obtained under a +10 volt gate bias are given in Table 1, and it is seen that V(sat) is more positive for the higher implantation energies.

The positive flat band voltage resulting from room temperature X-irradiation could be taken to negative values by prolonged exposure to 4.9 eV light under negative gate voltage conditions (Fig. 3). With this bias, electron injection from the semitransparent gold electrodes is small and most of the injected electrons are expected to be trapped in the displacement damage zone close to that electrode. The effect is therefore thought to be due to the photodepopulation of electrons trapped in the radiation damage zone during the X-ray exposure. This is supported by the observation that, under the same conditions, the flat band voltage of an unimplanted sample always shifts from its initial negative value towards zero.

At liquid nitrogen temperatures there was a net <u>positive charge</u> storage in the implanted oxide under all positive gate bias conditions (Fig. 2). Photodepopulation measurements indicated that this positive charge corresponded to the additional low temperature charge stored in the unimplanted oxide at 80°K, since it could be removed by illuminating the sample with photons of energy less than 2.5 eV. Under photodepopulation conditions at 80°K the flat band voltage shift could be reduced to zero by about 20 mins. illumination and taken to positive values by longer illumination. These measurements clearly indicate that charge compensation processes are involved in the radiation response of an implanted oxide.

c. Annealing of Implantation Associated Damage

In order to study the annealing of traps associated with the implanta-

tion of Al ions into the SiO, matrix and the associated negative charge storage in these oxides, MOS capacitors were annealed in a vacuum ambient for 30 mins. at a series of temperatures between 100° and 500° C. After each anneal the saturated flat band voltage produced by subsequent room temperature X-irradiation was measured for gate biases of +4 and +10 volts. Spot checks were made on V(sat) obtained under negative bias conditions. Fig. 4 shows the data obtained under positive gate bias. It is seen that the amount of negative charge stored in the oxide decreased as the annealing temperature increased and that V(sat) changed sign as higher annealing temperatures were reached, the fully annealed oxide storing net positive charge. The temperature at which V(sat) changed sign was seen to be gate voltage dependent, indicating that it is not just the number of traps but their state of occupancy that is important in determining V(sat). If the change in V(sat) at the 4 volt gate bias produced by an anneal at a given temperature is expressed as a fraction of the corresponding shift measured with a 10 volt gate bias, the fraction is found to be a constant, independent of the anneal temperature, having a value equal to the ratio of the gate biases. This suggests that the reduction of the bulk oxide field to zero by the trapped charges is important in determining the equilibrium trap occupancy and hence V(sat).

In addition to these isochronal measurements some samples were annealed isothermally so that activation energies associated with the annealing of the lattice displacement damage could be obtained. Preliminary results indicate that an energy of $1.2 \pm 0.1 \text{ eV}$ is associated with the annealing of the displacement damage. Electron photoinjection experiments on the annealed samples indicate that both bleaching of the electron traps and annealing of the displacement damage is occurring during the thermal treatment.

d. Scanning Electron Microscope Studies

Some MOS capacitors have been examined using the electron beam of a scanning electron microscope as a radiation source. By controlling the energy of the incident electron beam it is possible to create electron/hole

pairs at various depths within the oxide. The samples were mounted in such a way that capacitance-voltage and conductance-voltage measurements could be made in the microscope. In this series of measurements the sample was exposed to a predetermined number of electrons (9 x 10¹³/cm²) at a given energy and then the flat band voltage and conductance measurements were made to determine the oxide charge storage and the density of interface states (8). The electron beam energy was then increased in 100 volt steps and the procedure repeated until the beam penetrated through the oxide to the silicon. The gate electrode was grounded during these irradiations and the bias on the oxide was controlled by altering the potential of the silicon substrate. Preliminary results, obtained with implanted and unimplanted samples having 200 A semitransparent gold gate electrodes, are shown in Fig. 5. The substrate bias of -10 volts during the irradiation implies that electrons were attracted towards the gate electrode and holes to the Si/SiO₂ interface.

For the unimplanted sample, the flat band voltage was seen to increase linearly with electron beam energy until the beam penetrated the gold electrode and deposited energy directly in the SiO₂.

At this point the flat band voltage remained at the same value independent of beam energy. The implanted sample had an initially negative flat band voltage that corresponded to about 10% of the charge introduced into the oxide by the Al⁺ ions. While the electron beam lost all of its energy in the gold gate electrode there was essentially no change in the flat band voltage. Once the beam penetrated to the SiO₂ negative charge was stored in the oxide, the initial positive charge being largely annihilated or compensated for by the time the beam penetrated to the Si/SiO₂ interface.

Because of the strong interaction between the electron beam and the gold gate electrode, depth resolution was not high in these measurements and X-ray photons generated in the gold also played a role in the oxide charge storage and interface state generation processes.

Figure 6 shows the dependence of the interface state density on the energy of the incident electron beam. The total electron flux is the same for each data point. It is seen that with the electrons stopping in the gate electrode or within the displacement damage zone of the oxide, the number of interface

states remains constant at the pre-irradiation level. Once the beam starts to penetrate the relatively undamaged SiO_2 , interface state generation begins. The rate of interface state generation seems to increase once the electron beam reaches the interface and penetrates the Si substrate.

DISCUSSION

The data presented above indicate that Al implantation has a considerable effect on the saturated flat band voltage shift produced when an MOS capacitor is exposed to ionizing radiation under positive gate bias conditions, but only a small effect when the same device is irradiated under a negative bias. The fact that the implantation process can cause a net negative charge storage in an unannealed oxide at room temperature and that the trap levels associated with this charge storage anneal in the same temperature range in which optical, and E.S.R. absorption peaks associated with the implantation process also anneal (9), suggests that the electron traps are associated with the displacement damage created during implantation, rather than with chemical effects due to the addition of Al + ions to the matrix. This contention is supported by similar observations made by Emms et al. (10) where the implantation associated oxide modifications were found to be essentially independent of the implanting ion type. The data also suggest that the saturated flat band voltage shift is determined by that amount of charge which has to be stored in the oxide to reduce the bulk field to zero during X-irradiation, rather than on the number of new traps introduced during implantation. This follows from the relative independence of V(sat) under positive gate bias conditions on the total number of implanted ions, a condition that obtains both before and after thermal annealing of these samples. The spatial distribution of these traps is important in determining the value of V(sat) at a given gate bias as was indicated in Table I. It is also apparent that the major effect of the implantation is to provide compensatory electron traps in the oxide rather than providing electron/hole recombination paths. This is indicated by those experiments in which electrons were photodepopulated from the implantation associated traps by illuminating with 4.9 eV light under negative gate bias and the absence of a similar response in the unimplanted sample. This interpretation is supported by the low temperature data on the unannealed sample where the additional hole traps in the $\mathrm{SiO}_2/\mathrm{Si}$ interface region that become stable at $80^{\circ}\mathrm{K}^{(6)}$ more than counteracted the electrons trapped in the bulk displacement damage zone and produced a negative flat band voltage shift. Holes in these traps could then be removed by photodepopulation and the flat band voltage made to change sign.

The qualitative features of charge storage in the implanted oxide under both positive and negative gate bias are understandable in terms of a simple model in which it is assumed that the major effect of a shallow ${\rm Al}^+$ implantation is to produce a zone of displacement damage within the oxide that can trap a high density of electrons and holes. As indicated schematically in Fig. 7, the unimplanted oxide is assumed to be essentially free of electron traps $^{(11)}$ and to have hole traps largely concentrated in the interface regions at the gate and silicon electrodes $^{(12)}$. In the implanted oxide the hole traps at the ${\rm Si/SiO}_2$ interface are assumed to be similar in number to those in the unimplanted oxide and additional hole and electron traps are associated with the displacement damage zone generated by the implantation. This approximation may not be completely correct if the ionization produced during the implantation process creates new hole traps at the interface.

When the oxides are exposed to X-rays it is assumed that electron-hole pairs are generated uniformly throughout the oxide. Electron injection from the Si is ignored. In the displacement damage zone these carriers are expected to have a short mean free path before trapping in fields on the order of those encountered in device applications and would, therefore, charge compensate each other or recombine. In the relatively undamaged zone of the oxide, between the tail of the implantation profile and the silicon interface, both electrons and holes are assumed to be mobile and those which escape geminate recombination will move under the influence of the local field. It is assumed that the number of free electrons and holes depends linearly upon the oxide field for fields below circa 10⁶ volts cm⁻¹. On the basis of the data of Powell and Debenwick and Srour et al. (13) it is assumed that electrons are not trapped at the Si/SiO₂ interface but that some fraction, c, of the incident holes is trapped at this interface. Typically c has a value

of 10 \rightarrow 15%. Electrons or holes incident on the radiation damage zone of the oxide are assumed to be completely trapped in a region extending from x = a to x = (a+b), where x is measured from the metal insulator interface. This zone of the oxide will, therefore, have a net positive or negative charge at the end of a radiation exposure depending upon the sign of the gate voltage applied during irradiation. In the unannealed oxide there are assumed to be more traps in this damage region than are occupied by electrons or holes in the saturated flat band condition (when the field across the unimplanted region of the oxide has been reduced to zero by the trapped charges at its boundaries.

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Under positive gate voltage conditions the numbers of trapped holes and electrons on the basis of this model are given by

$$\int_{a}^{a+b} N^{-} dx = \int_{0}^{t} J_{e} dt$$

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and

$$\int_{\mathbf{x}_0 - \mathbf{d}}^{\mathbf{r}^+} d\mathbf{x} \approx C \int_{\mathbf{h}}^{\mathbf{t}} d\mathbf{t}$$
 (1)

where N and P are the density of trapped electrons and holes at the end of a radiation exposure of duration, t. J_e and J_h are the electron and hole fluxes and the quantities a, b, x_o and d are as defined in Figure 7. For this gate bias the electrons are trapped in the displacement damage zone and the holes at the Si/SiO₂ interface.

The electron and hole fluxes are linearly dependent upon the field in the undamaged part of the oxide and:

$$J_{e} = J_{h} = AE(x = a+b)$$
 (2)

where A is a constant depending upon the carrier generation rate and the geminate recombination parameters and:

$$E(x=a+b) = \left(\frac{V_g}{x_o}\right) - \left(\frac{p^+}{\varepsilon} \frac{d^2}{2x_o}\right) - \left(\frac{N^-}{\varepsilon} \frac{(2ab + b^2)}{2x_o}\right)$$
(3)

where ϵ is the dielectric constant of the ${\rm SiO}_2$. Using these relationships, expressions may be developed for the rate of filling of electron and hole traps. These have the form

$$\frac{dP^{+}}{dt} = \frac{cA}{d} \left(\frac{V_g}{x_o} - \frac{1}{2\varepsilon x_o} \left[P^{+} d^2 + V^{-} (2ab+b^2) \right] \right)$$
 (4)

and

$$\left(\frac{dN^{-}}{dt}\right) = \left(\frac{d}{bc}\right)\left(\frac{dP^{+}}{dt}\right)$$

The flat band voltage as a function of radiation time is then given by:

$$V_{FB} = -\frac{1}{\varepsilon} \int_{x_0-d}^{x_0} P^+(t) dx + \frac{1}{\varepsilon} \int_{a}^{a+b} x N^-(t) dx$$
 (6)

and substituting for $P^+(t)$ and $N^-(t)$ obtained from equations (4) and (5) using Laplace transform techniques and evaluating the integrals of Eq. (6) gives

$$V_{FB} = V_{g} \left[1 - \frac{2x_{o}c}{cd+(2a+b)} \right] \left(1 - exp - \left\{ \frac{Bt}{x_{o}} \right\} \right)$$
 (7)

where B is a constant for given radiation conditions. As t $\rightarrow \infty,$ V_{FB}^{-+} V(sat) and so

$$V(sat) = V_g \left[1 - \frac{2x_o c}{cd+(2a+b)} \right]$$
 (8)

The values of a and b are dependent upon the energy of the implanting ions. In order to compare the predictions of this model with the data obtained at different implantation energies, a and b have been related to numerical data (14) on the projected range, R, and standard deviation, σ , of the implantation profile. Using a = (R-2 σ) and b = 4σ the expression for V(sat) can be simplified to give

$$V(sat) = V_g \left[1 - \frac{2x_o c}{cd + 2R}\right]$$
 (9)

Using $x_0 = 1315$ Å, d = 300 Å, c = 0.1 and $V_g = 10$ volts, V(sat) can be computed for various implantation energies. These values are shown in Table I together with the projected range and standard deviation of the implantation profile. Considering the simplicity of the model the agreement with experiment is surprisingly good. Eq. (9) also indicates that there is an optimum projected range for producing a hard oxide when sufficient electron traps are available. For V(sat) = 0

$$R = c(x_0 - d/2) \tag{10}$$

Under negative gate bias all those electrons escaping geminate recombination will enter the silicon as it has been assumed that the undamaged oxide has no electron traps. The holes will be trapped in the trailing edge of the displacement damage zone between a and a+b. Carrier separation will continue until the field in the undamaged region of the oxide goes to zero because of the trapped hole charge. For this case:

$$\int_{a}^{a+b} P^{+} dx = \int_{0}^{t} J_{h} dt$$
 (11)

also $J_h = J_e = AE$ where

$$E = \frac{V_{\mathbf{g}}}{x_{0}} + \frac{P^{+}}{\varepsilon} \frac{(2ab + b^{2})}{2x_{0}}$$
 (12)

and the final number of trapped holes is given by

$$P^{+} = \frac{-2\varepsilon V_{g}}{(2ab+b^{2})} \tag{13}$$

under which condition $V(\text{sat}) = V_g$ and oxide hardening is not possible. Again the prediction of the model is in reasonable agreement with experiment. Any electron trapping within the oxide, such as may occur at low temperatures, would be expected to make V(sat) under negative gate voltage conditions less negative.

The thermal annealing experiments indicate that the implantation associated displacement damage anneals with an activation energy of 1.2 ± 0.1 eV. The thermal depth of electron traps induced in SiO_2 by implantation with Au ions has been determined by Chen et al. (15) to be essentially the same value. If these electron traps are associated with displacement damage, as is suggested by the present experiments, then both bleaching of the electron traps and their annealing by lattice recombination processes will occur in the same temperature range. The electron photoinjection experiments indicate that this is the case.

The flat band voltage behavior of the samples examined in the S.E.M. also indicates that the implant zone of the oxide is a source of traps for both electrons and holes. Electron-hole pairs generated by the electron beam stopping in this region either recombine or are trapped in approximately equal numbers. Once the electron beam penetrates beyond this region of high trap density those electron-hole pairs generated in the relatively undamaged region of the oxide may be separated by the applied field. A fraction of the holes incident upon the SiO₂/Si interface is trapped and create interface states. The electrons incident upon the damage zone are largely trapped and serve to charge compensate the holes at the Si/SiO₂ interface.

The creation of interface states by the hole flux is suggested by the data of Fig. 6. In the implanted sample the number of these states remains relatively constant until the electron beam penetrates beyond the maximum of the implantation damage region. Hole transport to the $\mathrm{SiC}_2/\mathrm{Si}$ interface can then occur and the interface state density increases with increasing

electron beam irradiation. In the unimplanted sample, where holes are assumed to be essentially free whereever they are generated, the number of interface states increases linearly with electron beam penetration into the oxide and remains approximately constant once the beam has penetrated to the SiO_2/Si interface.

Charge coupled devices are of interest for use as imaging systems in an "integrated focal plane". Killiany et al. (16) have shown that considerable image degradation may occur when such CCD's are exposed to as little as 10 rads. These authors suggest that standard MOS hardening techniques can be used to make a substantial improvement in the device hardness to ionizing radiation. The present measurements indicate that while this may be true at room temperature, devices cooled to low temperatures to increase their photon detection sensitivity cannot be satisfactorily radiation hardened by the same implantation technology that increases device radiation resistance at room temperature. Thermally stimulated current data indicates that the additional hole traps responsible for the low temperature oxide "softness" become unstable at circa 150K. Some cooling of the CCD structure should therefore be possible before these traps contribute to the device radiation sensitivity.

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TABLE 1.

Implantation Energy (KeV)	10	20	30
Fluence. (cm ⁻²)	10 ¹⁵	10 ¹⁴	10 ¹⁵
V(sat) exptl. (volts)	3.0	5.5	7.0
R. (Å)	140	270	400
σ (Å)	45	80	110
V(sat) theor.	1.5	5.4	6.9

A comparison between the calculated and experimental saturated flat band voltages for implanted MOS capacitors.

FIGURE CAPTIONS

- Fig. 1. Saturated flat band voltage as a function of gate voltage during X-irradiation for an unimplanted sample.
- Fig. 2. Saturated flat band voltage as a function of gate voltage during X-irradiation for an implanted sample (10¹⁴ Al cm⁻²: 20 KeV).
- Fig. 3. Photodepopulation of trapped electrons in an unannealed sample following room temperature X-irradiation under positive bias. $(10^{15} \text{ Al cm}^{-2}: 30 \text{ KeV}).$
- Fig. 4. Saturated flat band voltage measured at room temperature as a function of the annealing temperature of an implanted sample.
- Fig. 5. Flat band voltages of MOS capacitors of a function of electron beam energy for unimplanted and implanted samples.
- Fig. 6. Interface state generation as a function of electron beam energy in implanted and unimplanted samples.
- Fig. 7. Models for electron and hole trapping in unimplanted SiO₂ MOS structures.

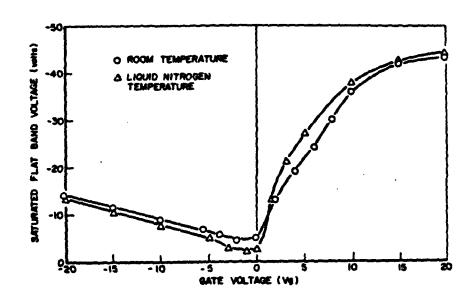


Figure 1

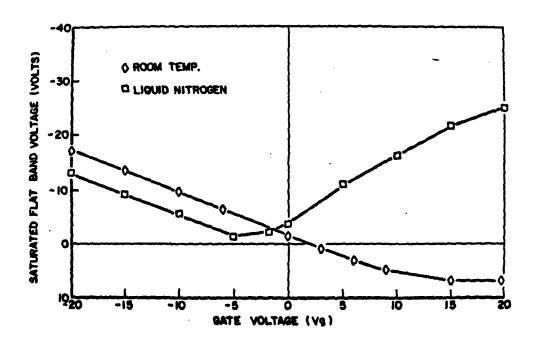


Figure 2

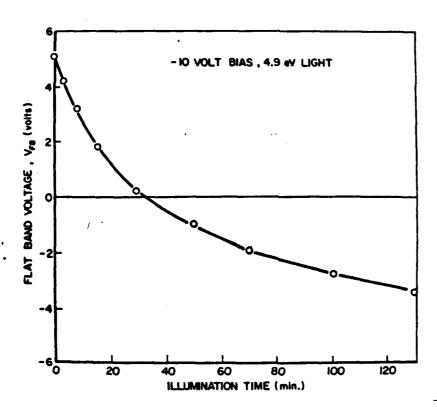
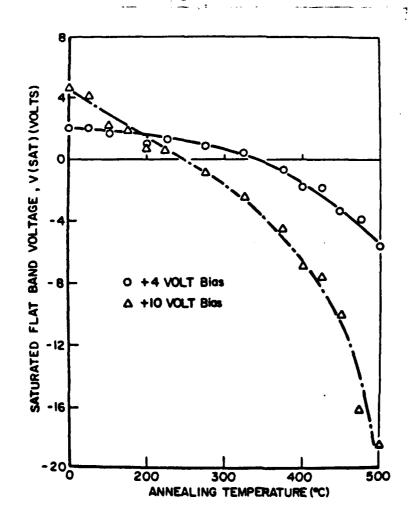


Figure 3



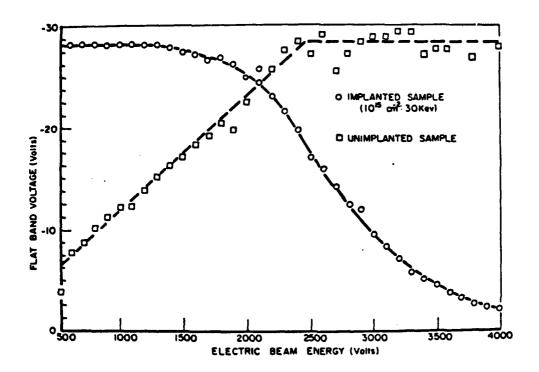


Figure 5

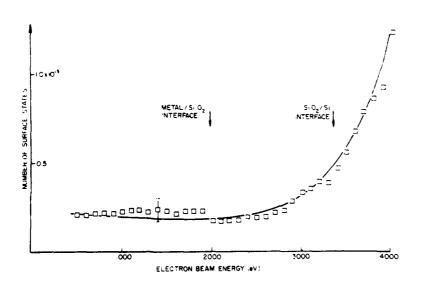
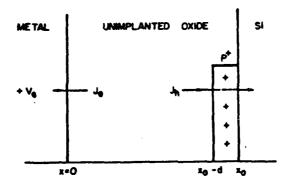


Figure 6



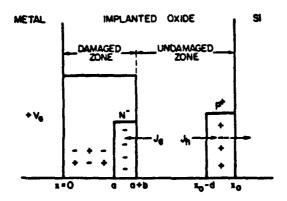


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